

Description**Field of the Invention**

[0001] This invention relates to demodulation methods and particularly but not exclusively to methods for demodulating a Radio-Frequency (RF) signal in a portable communications device.

Background of the Invention

[0002] Portable communications devices such as mobile telephones typically operate with a limited power supply in the form of a battery, and hence have a limited period of operation before the battery must be recharged or replaced.

[0003] Many efforts are being made to reduce the power consumption of such portable devices, in order to lengthen the above period of operation. When such a portable device is not actively involved in a call, (a so-called standby mode), the device periodically 'listens' to a control channel, which will then alert the device in the case of an incoming call. This is referred to as Discontinuous Receiving Mode (DRX mode). During DRX mode, most power is consumed when the receiver apparatus is actually switched on, and therefore a key goal is to reduce the receiver apparatus 'on' time.

[0004] A problem with the receiver apparatus is that whilst receiving and demodulating a signal, Direct Current (DC) interference generated internally interferes with the signal, limiting dynamic range.

[0005] A known solution to this problem is to provide in the receiver apparatus, a DC adapt step, prior to demodulating the signal, which substantially cancels the DC interference. However the receiver apparatus must be switched on during this DC adapt step, thereby causing an increased 'on' time of the receiver apparatus and hence resulting in a large power drain.

[0006] This invention seeks to provide a demodulation method which mitigates the above mentioned disadvantages.

Summary of the Invention

[0007] According to a first aspect of the present invention there is provided a demodulation method for demodulating a radio frequency signal having a first frequency, comprising the steps of: oscillating demodulation means at a second frequency, the second frequency being different from the first frequency; measuring a DC offset value from the second frequency, the DC offset value being associated with internal interference; oscillating the demodulation means at the first frequency in order to demodulate the radio frequency signal, thereby providing a demodulated signal; subtracting the DC offset value from the demodulated signal in order to provide a demodulated signal with a substantially reduced DC component; monitoring the

demodulated signal for further DC offset components; and subtracting the further DC offset components from the demodulated signal.

[0008] According to a second aspect of the present invention there is provided a demodulation arrangement for demodulating a radio frequency signal having a first frequency, the arrangement comprising: demodulation means arranged to oscillate at the first frequency and at a second frequency, the second frequency being different from the first frequency; filtering means for measuring a DC offset value from the first frequency and from the second frequency, the DC offset value being associated with interference; and subtracting means for subtracting the DC offset value from the demodulated signal in order to provide a demodulated signal with a substantially reduced DC component, wherein the demodulation means initially oscillates at the second frequency such that the filtering means measures a DC offset value substantially dependent upon internal interference.

[0009] In this way a demodulation method and arrangement are provided which exhibit reduced power consumption by providing a short DC adapt step which reduces the 'on' time of the receiver (demodulator).

Brief Description of the Drawings

[0010] An exemplary embodiment of the invention will now be described with reference to the drawing in which:

FIG. 1 shows a preferred embodiment of a receiver of a portable communications device in accordance with the invention.

FIG. 2 shows a detailed view of a portion of the embodiment of FIG. 1.

FIG. 3 shows a series of frequency diagrams illustrating signals associated with the invention.

FIG. 4 shows an alternative embodiment of a receiver of a portable communications device in accordance with the invention.

Detailed Description of a Preferred Embodiment

[0011] Referring to FIG. 1, there is shown a RF Direct Conversion Receiver (DCR) 5 of a portable communications device. The DCR 5 has an antenna 7, coupled via a receive filter 8 to an amplifier and mixer stage 10, and a low frequency stage 100.

[0012] The amplifier and mixer stage 10 has a low noise amplifier with an input coupled to receive a filtered RF signal from the receive filter 8 and an output which is split into two paths. A first path is coupled via a first mixer 30 to a first signal amplifier 40. Similarly a second path is coupled via a second mixer 50 to a second sig-

nal amplifier 60.

[0013] The first and second mixers 30 and 50 are also coupled to receive sine and cosine components respectively of an oscillating signal from a fractional-N type synthesised oscillator 70. In this way the first and second mixers 30 and 50 and the first and second signal amplifiers 40 and 60 respectively provide in-phase (I) and quadrature (Q) mixed signals which are demodulated components of the RF signal.

[0014] First and second Digital-to-Analogue Converters (DACs) 35 and 55 provide static offset values for the first and second mixers 30 and 50 respectively, to be further described below. Further DACs 75 provide phase and mismatch correction functions for the fractional-N oscillator 70, via a CR/RC network 77. The CR/RC network is a quadrature network generator that generates cosine and sine components of the fractional-N oscillator 70. The first and second signal amplifiers 40 and 60 each have gain control inputs, for adjusting the gain thereof.

[0015] The low frequency stage 100 also has two paths. A first path, which starts from the I signal of the first signal amplifier 40 (the I path) comprises (in sequence) a first bandwidth adjustment filter 110, a first low-frequency amplifier 120, a first Analogue-to-Digital (A/D) converter 130 and a first baseband filter 140. The output of the first baseband filter 140 is a signal $Id(t)$.

[0016] Similarly the second path, which starts from the Q signal of the second signal amplifier 60 (the Q path) comprises (in sequence) a second bandwidth adjustment filter 160, a second low-frequency amplifier 170, a second A/D converter 180 and a second baseband filter 190. The output of the second baseband filter 190 is a signal $Qd(t)$.

[0017] The first and second bandwidth adjustment filters 110 and 160 and the first and second baseband filters 140 and 190 each have filter control inputs, to control the filtering thereof. Similarly the first and second low-frequency amplifiers 120 and 170 each have gain control inputs to control the gain thereof.

[0018] Referring now also to FIG. 2, which shows in greater detail a portion of the low frequency stage of FIG. 1, there is provided a gain/phase correction block 200 and a complex low-pass filter (LPF) 210.

[0019] The gain/phase correction block 200 is coupled to receive the $Id(t)$ and $Qd(t)$ signals and Gain adjustment (Ad) and Phase (ϕ) control signals. The block 200 may be realised in hardware or software, and is arranged to provide the following result:-

$$Iout+jQout=Id+jQd*Ad*ej(\phi) \quad \text{Equation 1}$$

where $Iout$ and $Qout$ are gain corrected, phase adjusted I and Q signals. The Ad and ϕ control signals are factory set, and are intended to remove any phase or gain mismatches occurring between the I and Q paths as a result of analogue device variations. Any such mismatches could cause aliasing between channels of the

receive spectrum.

[0020] The $Iout$ and $Qout$ signals are then filtered by the complex LPF 210 to produce IDCest and QDCest signals representing the DC offset component of the $Iout$ and $Qout$ signals. The IDCest signal is then subtracted from the $Iout$ signal, at a mux block 220. Similarly, the QDCest signal is subtracted from the $Qout$ signal, at a mux block 230. In this way the DC offset component of the $Iout$ and $Qout$ signals are substantially cancelled.

[0021] In operation, and referring now also to FIG. 3, a fast DC adapt step is achieved as follows. For desired demodulation of a frequency f , the fractional-N oscillator 70 is first set to a frequency $F=f+\delta$, where δ is an appropriate offset value. In FIG. 3a, there is shown a wanted spectrum 300 centred on the frequency f , and an adjacent channel spectrum 310. Gain and phase mismatches between the I and the Q paths result in aliased images of the wanted spectrum 300 and the adjacent channel spectrum 310, which appear as images 315 (image of the wanted spectrum 300) and 305 (image of the adjacent channel spectrum 310). The offset δ is chosen in this case to be half of the bandwidth of the wanted spectrum 300, such that the initial oscillation frequency F ($=f+\delta$) is outside of the wanted spectrum 300, and also clear of the adjacent channel 310. A vector $Vin(t)$ at the frequency F , represents the DC offset derived from $Id(t)$ and $Qd(t)$.

[0022] FIG. 3b shows a second vector $Vout(t)$ (derived from $Iout$ and $Qout$) representative of the gain and phase corrected DC offset. The gain and phase correction substantially removes the images 305 and 310 from the adjacent channel 310 and the wanted spectrum 300 respectively. A wideband envelope 350 of FIG. 3b represents the wideband filtering to be performed by the complex LPF 210. FIG. 3c then shows the result of this filtering, in the form of a third vector $VDC(t)$ (derived from IDCest and QDCest) which represents the DC offset.

[0023] The DC offset value is based on a measurement shifted from the frequency f , and is therefore almost exclusively the result of internal interference. Also, it is possible during the fast DC adapt mode, to effectively switch off the amplifier and mixer stage 10, by switching off or reducing the gain of the LNA 20 in order to reduce the levels of wanted signals and adjacent channels versus the DC offsets. This RF isolation is of interest during the static DC offset value estimation.

[0024] The fractional-N oscillator 70 is then set to oscillate at the frequency f , in order to provide the desired demodulated signal. The DC offset value given by IDCest and QDCest is then subtracted from the demodulated signal in order to provide a demodulated signal with a substantially reduced DC component.

[0025] The blocks 200 and 210 then continue to provide further DC offset values, which are subtracted to further reduce the amount of DC offset present in the demodulated signal. However, the complex LPF 210

may be adjusted so as to have a different filter envelope to the wideband envelope 350 shown in FIG. 3b. In particular, the complex LPF 210 may, when filtering the demodulated signal, define a narrowband envelope.

[0026] The first and second DACs 35 and 55 may be arranged to store the results of the fast DC adapt step described above, such that when the same wanted frequency is demodulated at a later time, the DACs 35 and 55 can provide appropriate static offset values for the first and second mixers 30 and 50 respectively, such that the fast DC adapt step need not be performed every time the wanted frequency is demodulated.

[0027] Referring now also to FIG. 4, there is shown a zero-IF (ZIF) RF receiver 400 of a portable communications device. The ZIF RF receiver 400 differs from the DCR receiver 100 of FIG. 1 in that the demodulation takes place in two stages, and there are two oscillators. A first stage 410 comprises a main synthesiser 420, which demodulates a received signal to an intermediate frequency (IF).

[0028] The second stage 500 has a second oscillator 510, which is a low-order fractional-N synthesiser, coupled to provide oscillation signals to first and second mixers 520 and 530. The first and second mixers 520 and 530 split the IF signal from the first stage 410 into two paths, an I path and a Q path, similar to those of FIG. 1. The use of a similar approach to DCR in ZIF receiver 400 as in DCR is possible. However, a different type of cancellation is required for the ZIF receiver 400.

[0029] The IF signal will always be at the same frequency (the intermediate frequency) and therefore the second oscillator 510 need only have two oscillation frequencies; the IF (for demodulation) and $IF + \delta$ (for the DC adapt step). During the fast DC adapt, the second oscillator 510 is shifted in frequency to $IF + \delta$.

[0030] The DC adapt is performed by a number of DC adapt blocks. DC adapt feedback blocks 520, 530, 550 and 560 are coupled to provide DC offset feedback cancellation for amplifiers 525, 535, 555 and 565.

[0031] The DC adapt block 550 estimates the DC offsets of the first stage 410 through the use of a low pass filter (in a wideband configuration). This estimated DC offsets is compared to zero. The resulting error is integrated by an integrator and feedback to the input of the amplifier 555. This forms a DC adapt loop which will converge to zero DC output after a response time.

[0032] After the fast DC adapt step is performed, the second oscillator 510 switches to the IF and the low pass filter of the DC adapt block 550 is set to a narrowband configuration to continue to estimate the DC offsets variation.

[0033] The other DC adapt blocks 520, 530 and 560 operate in a similar way, and serve to increase the Dynamic range of each associated amplifier (525, 535 and 565) by substantially cancelling the associated DC offsets.

[0034] Analogue DC adapt blocks 540 and 570 are also provided for the I and Q paths respectively, and

these are required in the case that A/D converters 575 and 545 do not have enough dynamic range to accept amplified DC offsets present in the analogue signal.

[0035] It will be appreciated that alternative embodiments to the one described above are possible. For example, the value of the frequency shift δ may be different from that given above.

[0036] Furthermore, the complex LPF 210 could be replaced by one or more filters with different attributes, which result in substantially the same DC offset value.

Claims

1. A method for demodulating a radio frequency signal having a first frequency (f), comprising the steps of:

20 oscillating demodulation means at a second frequency (F), the second frequency (F) being different from the first frequency (f);
 measuring a DC offset value from the second frequency (F), the DC offset value being associated with internal interference;
 25 oscillating the demodulation means at the first frequency (f) in order to demodulate the radio frequency signal, thereby providing a demodulated signal;
 subtracting the DC offset value from the demodulated signal in order to provide a demodulated signal with a substantially reduced DC component;
 30 monitoring the demodulated signal for further DC offset components; and
 subtracting the further DC offset components from the demodulated signal.

35 2. The method of claim 1, wherein the step of measuring the DC offset value at the second frequency (F) is performed by wideband low-pass filtering means and the step of monitoring the demodulated signal for further DC offset components is performed by a narrowband low-pass filtering means.

40 3. The method of claim 2, wherein the wideband and narrowband low-pass filtering means are provided by a single low-pass filtering means having a narrowband and a wideband mode.

45 4. The method of claim 2 or claim 3, wherein each of the low-pass filtering means is a complex filter.

50 5. The method of any preceding claim, further comprising the steps of:

55 isolating the demodulation means from the radio frequency signal during the step of oscillating the demodulation means at the second frequency (F);
 measuring a static DC offset value which is

substantially only the internal interference of the demodulation means;
storing the static DC offset value in a storage means;
re-connecting the demodulation means to the radio frequency signal before the step of measuring the DC offset value from the second frequency (F). 5

6. The method of claim 5, further comprising the steps of: 10

substantially removing the static DC offset value from the DC offset value before the step of subtracting the DC offset value from the demodulated signal; and 15
independently subtracting the static DC offset signal from the demodulated signal.

7. The method of claim 5 or claim 6, further comprising the steps of: 20

measuring a static DC offset value for each of a number of configurations of the demodulation means; 25
storing the static DC offset values in a storage means; and
using the stored values in dependence upon the chosen configuration. 30

8. A demodulation arrangement for demodulating a radio frequency signal having a first frequency (f), the arrangement comprising: 35

demodulation means (70) arranged to oscillate at the first frequency (f) and at a second frequency (F), the second frequency (F) being different from the first frequency (f);
filtering means (210) for measuring a DC offset value from the first frequency (f) and from the second frequency (F), the DC offset value being associated with interference; and 40
subtracting means (220, 230) for subtracting the DC offset value from the demodulated signal in order to provide a demodulated signal with a substantially reduced DC component, wherein the demodulation means (70) initially oscillates at the second frequency (F) such that the filtering means (210) measures a DC offset value substantially dependent upon internal interference. 45 50

9. The method or arrangement of any preceding claim, wherein the second frequency (F) is chosen to be at a frequency associated with a point of substantially minimum spectral power density of a power spectrum associated with the first frequency (f). 55

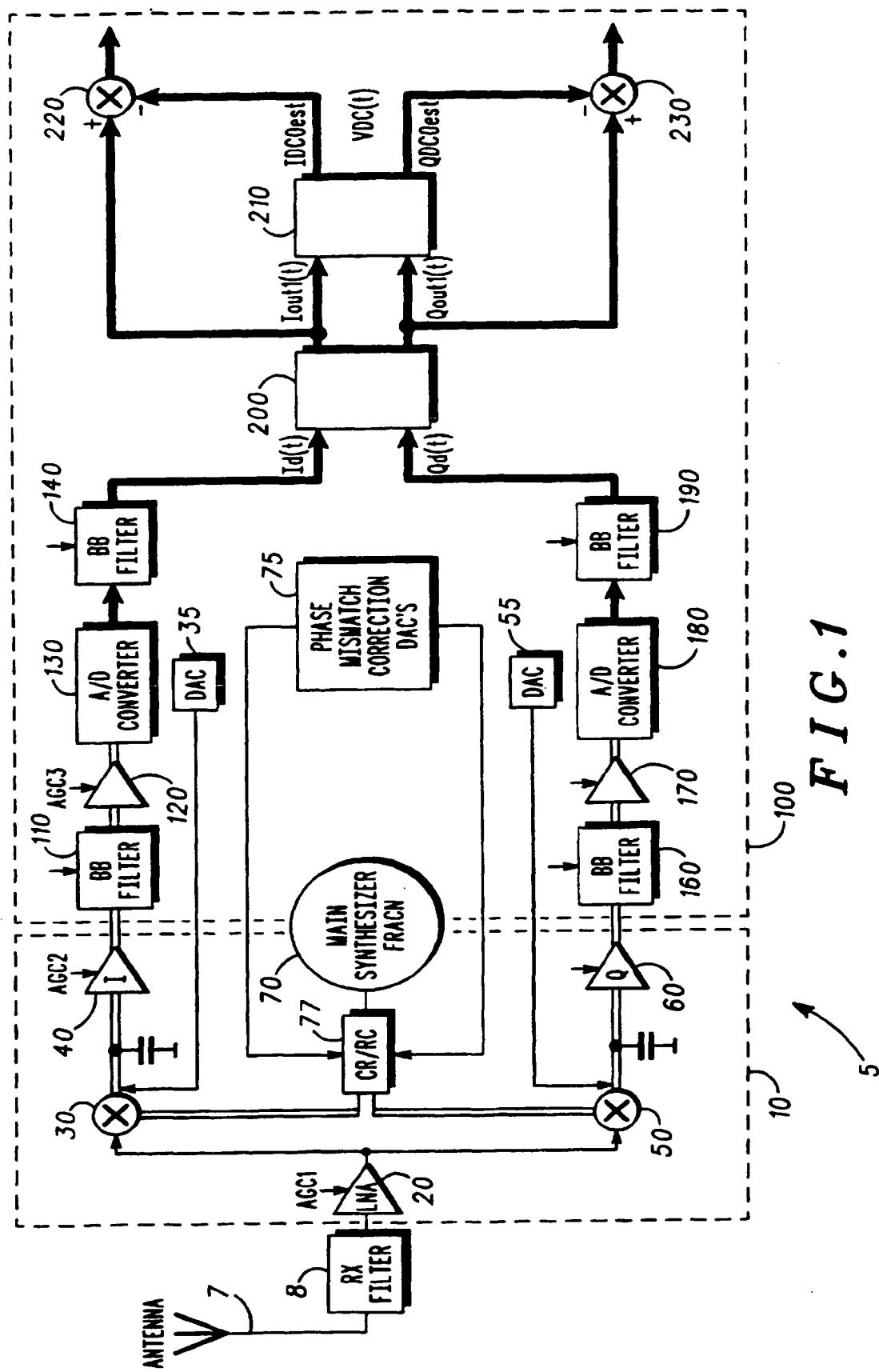
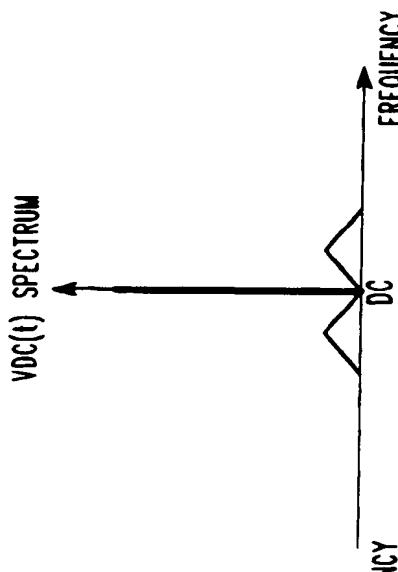
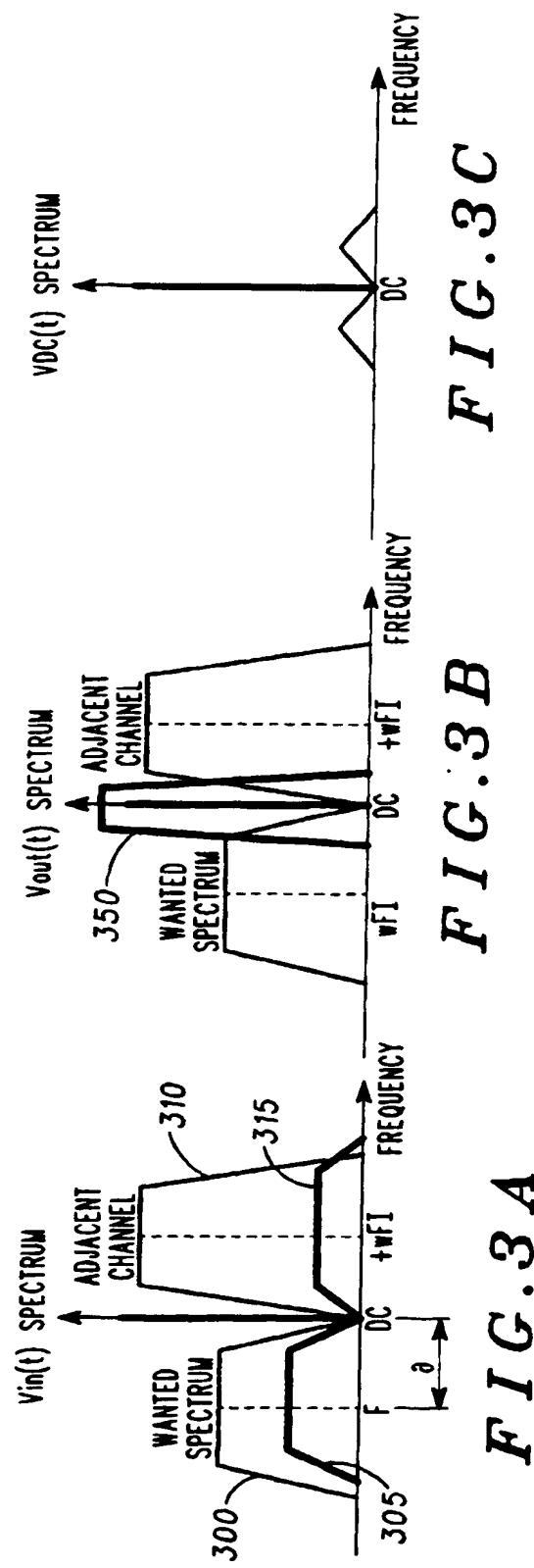
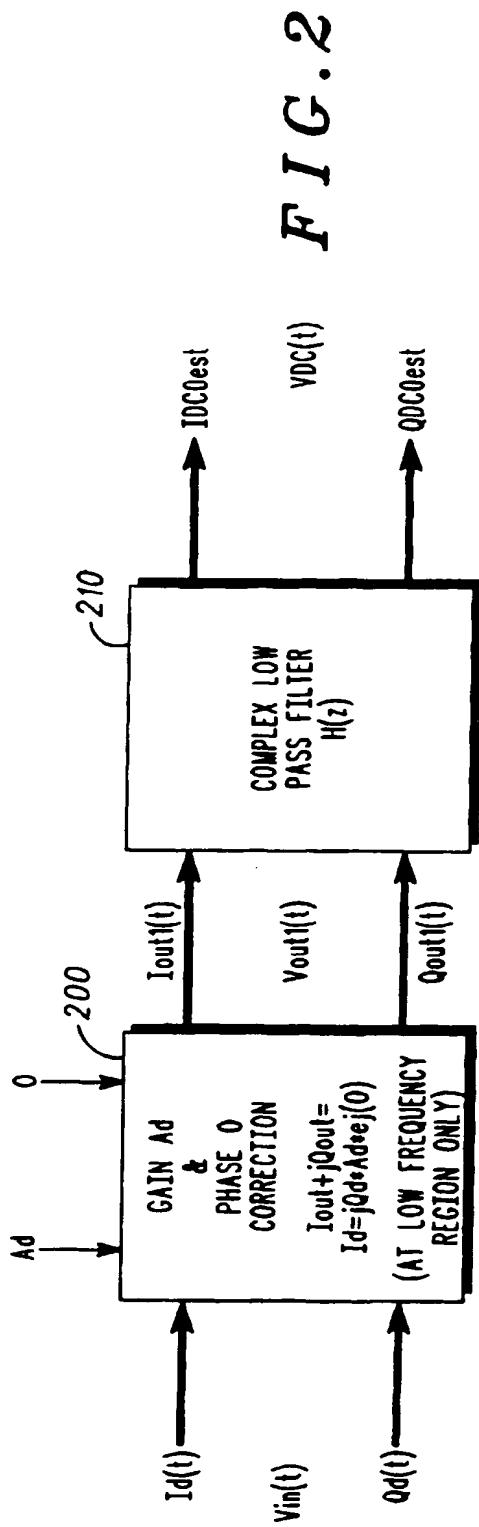


FIG. 1



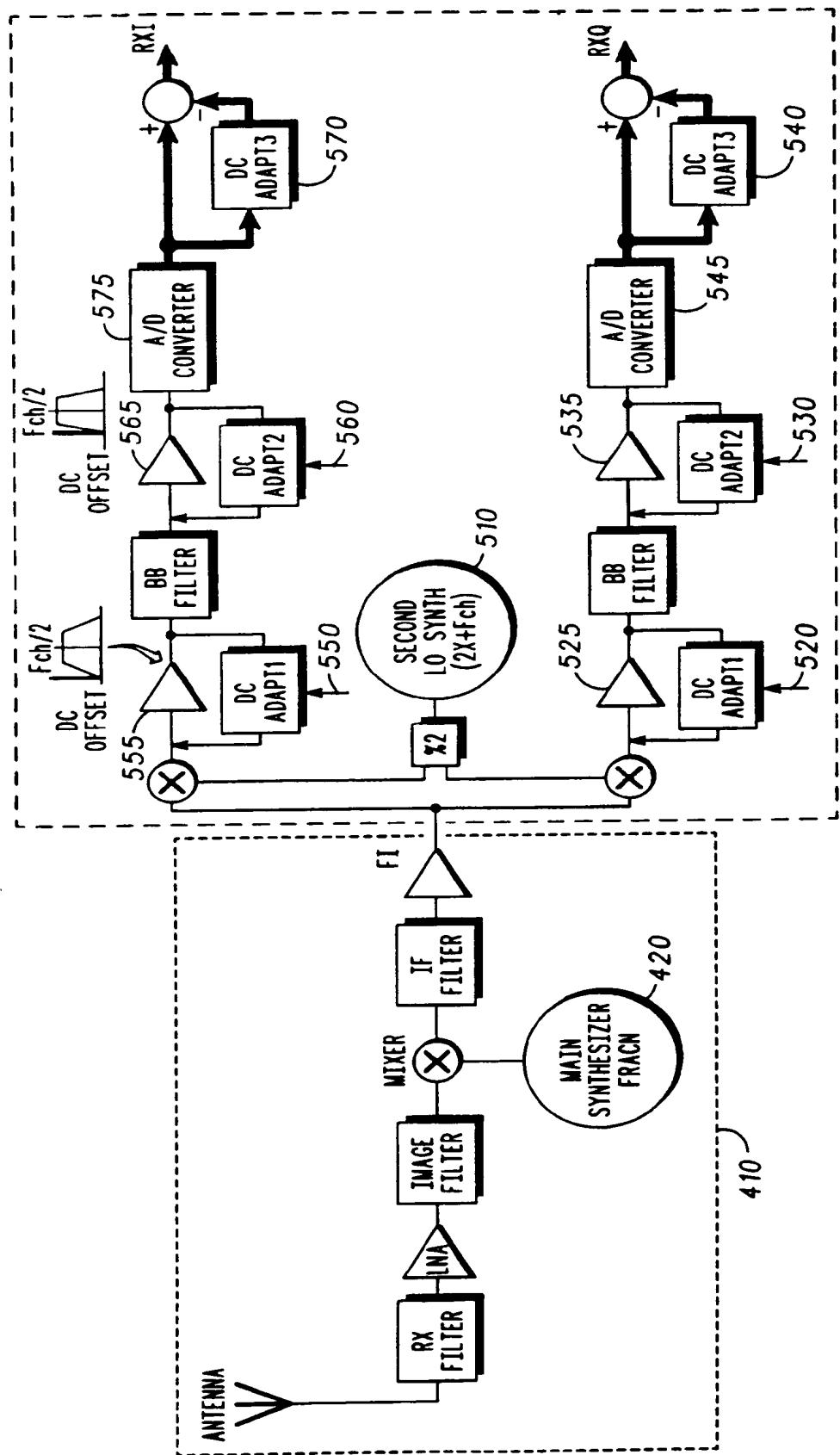


FIG. 4



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Application Number
EP 98 40 0807

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
X	US 5 548 244 A (CLEWER RICHARD) 20 August 1996 * abstract * * column 1, line 60 - column 2, line 34 * * column 3, line 31 - column 4, line 30 * ---	8-10	H03D3/00 H04L25/06
Y	US 5 212 826 A (RABE DUANE C ET AL) 18 May 1993 * abstract * * column 3, line 57 - column 4, line 51 * * column 5, line 9 - line 20 * ---	1-6	
A	EP 0 719 013 A (AT & T CORP) 26 June 1996 * abstract * * column 1, line 32 - column 3, line 8 * * column 5, line 45 - column 6, line 22 * * column 7, line 35 - column 8, line 32 * * column 9, line 42 - line 47 * -----	1-8	
The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H04L H03D
Place of search	Date of completion of the search		Examiner
THE HAGUE	28 September 1998		Koukourlis, S
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